



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/796,484	03/08/2004	Daniel Lee Avery	US 030078	2303
24738	7590	03/03/2006	EXAMINER	
PHILIPS ELECTRONICS NORTH AMERICA CORPORATION INTELLECTUAL PROPERTY & STANDARDS 1109 MCKAY DRIVE, M/S-41SJ SAN JOSE, CA 95131			TU, CHRISTINE TRINH LE	
		ART UNIT	PAPER NUMBER	
		2138		
DATE MAILED: 03/03/2006				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/796,484	AVERY ET AL.
	Examiner Christine T. Tu	Art Unit 2138

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 08 March 2004.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-25 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-25 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 08 March 2004 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ . |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ . |

Drawings

1. Figures 1-8 are objected to under 37 C.F.R. 1.84(o). All features represented by boxes in figures must be labeled with a function or a term which indicates what process or what element each box represents. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1, 2, 3, 4, 5, 6, and 9 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims (1, 2, 4), 7, 8, 9, 10, 11 and 3 of the copending Application No.10/796,480, respectively. Although the conflicting claims are not identical, they are not patentably distinct from each other because the copending application '480 substantially teaches the claimed invention. The copending application '480 does not explicitly teach the routing circuitry having test signal routing paths which is located inside a circuit configurator arrangement. However, the copending application '480 teaches the routing circuitry having test signal routing paths (in the preamble of claim 1 of copending application'480) . It would have been obvious to one skilled in the art to realize that the

circuit configurator arrangement of copending application '480 would be comprised of a routing circuitry having test signals routing paths instead. One having ordinary skill in the art would be motivated to realize so because having the routing circuitry being located inside or outside of the circuit configurator arrangement would have been a design choice and such a choice would not affect the functionality of the configurator arrangement.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

4. Claims (12 & 13), 14, 15 and 17 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 14, 15, 16 and 17 of the copending Application No.10/796,480, respectively. Although the conflicting claims are not identical, they are not patentably distinct from each other because the copending application '480 substantially teaches the claimed invention. The copending application '480 does not explicitly teach the configured circuit having plurality of controllable switches which is located inside a configurator arrangement. However, the copending application '480 teaches a configured circuit having plurality of controllable switches (in the preamble of claim 1 of copending application'480) . It would have been obvious to one skilled in the art to realize that the configurator arrangement of copending application '480 would be comprised of the configured circuit with the plurality of controllable switches instead. One having ordinary skill in the art would be motivated to realize so because having the configured circuit being located

inside or outside of the configurator arrangement would have been a design choice and such a choice would not affect the functionality of the configurator arrangement.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

5. Claims 19, 21 and 22 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 23, 26 and 27 of copending Application No. 10/796,480, respectively. Although the conflicting claims are not identical, they are not patentably distinct from each other because the copending application '480 teaches the claimed invention. The copending application '480 does not explicitly teach the configurator server. The copending application '480, however, teaches the configurator circuit. It would have been obvious to one skilled in the art at the time the invention was made to realize that the configurator circuit (as taught by the copending application '480) would have been named as "configurator server". One having ordinary skill in the art would be motivated to do so because naming the configurator circuit (of the copending application '480) as "configurator server" would not affect the functionality of the configurator circuit.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

6. Claims 24 and 25 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 29 of the copending Application No.10/796,480, respectively. Although the conflicting claims are not identical, they are not patentably distinct from each other because the copending application '480 substantially teaches the claimed invention. The copending application '480 does not explicitly teach the routing means having test signal routing paths which is located inside a circuit configurator. However, the copending application '480 teaches a routing circuitry having test signal routing paths (in the preamble of claim 29 of copending application'480) . It would have been obvious to one skilled in the art to realize that the circuit configurator arrangement of copending application '480 would be comprised of a routing circuitry/means having test signals routing paths instead. One having ordinary skill in the art would be motivated to realize so because having the routing circuitry/means being located inside or outside of the circuit configurator arrangement would have been a design choice and such a choice would not affect the functionality of the circuit configurator arrangement.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 112

7. Claims 1-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 2, 4, 12, 17-19, 21, 24:

The use of the phrase(s) "adapted to" (throughout the claims) should be avoided because such a phrase does not provide positive limitation but only has the ability to perform so. In other words, it is not clear whether or not any functional limitation is actually being recited after each phrase "adapted to".

Claim 4:

At lines 2-4, the phrase "the configured circuit includes a plurality of ... signal path switches adapted to route JTAG signals on the configured circuit and between the configured circuit and other configured circuits coupled to the configured circuit" cannot be understood. Firstly, it is not clear where exactly the JTAG signals should be routed (by signal path switches) to? To other configured circuits? Secondly, What does "other configured circuits coupled to the configured circuit" mean?

Claim 6:

The use of the words "separably" and "operable" (at line 2) should be avoided because it is not clear whether or not the microcontroller is ACTUALLY separated, and whether or not the microcontroller is ACTUALLY operating.

Claim 12:

At line 15, the term “the communications port” lacks antecedent basis. It is not clear where the communications port comes from.

At lines 16-17, the term “the microcomputer arrangement” lacks antecedent basis. It is not clear whether the term should be referring as “the hardware configurator arrangement” (as being recited at line 1).

Claim 13:

At line 4, it is not clear whether the term “at least one of the JTAG test nodes” should be replaced with –said one of the JTAG test nodes—since the microcontroller switches are controlled after being detected a test signal at one of the JTAG test nodes (as being recited at lines 2-3).

At line 4, the term “data” should be replaced with –said test signals—because consistent term should be used throughout all claims. In other words, the term should be consistent with the term “test signals” as being recited at line 17 of claim 12 (independent claim).

Claim 15:

At line2-3, the term “JTAG test data” should be replaced with –said test signals—because consistent term should be used throughout all claims. In other words, the term should be consistent with the term “test signals” as being recited at line 17 of claim 12 (independent claim).

It is not clear how the controllable switches can route any JTAG test data between the configured circuit and another configured circuit because the switches are only coupled to the target circuit devices and the two JTAG test nodes as being recited previously (at lines 2-4 of claim 12).

Claim 19:

It is not clear whether or not the configurator server (at lines 3-4) should be comprised of the inter-connectable circuit boards (at line 1) since part of the server (a reprogrammable microcontroller [at line 8]) is located on a ...first of the inter-connectable circuit boards (as being recited at lines 6-7).

Claim 20:

The term “the inter-connectable circuit arrangements” should be replaced with – the inter-connectable circuit boards— (as being previously recited at lines 2 of claim 19)because consistency of a term should be used throughout all claims.

Claim 23:

The term “the inter-connectable circuit arrangements” (at lines 1-2, 3-4 and 5) and the term “the ... inter-connectable circuit arrangements” (at lines 7-8) lack antecedent basis. The term should be replaced with “the inter-connectable circuit blocks” if the term is referring back to the inter-connectable circuit boards as being recited at line 1 of claim 19.

Claim 24:

At lines 8-9, the term “the routing circuitry” lacks antecedent basis. The term should be replaced with “the routing means” if it refers back to the routing means (as being recited at line 5).

Claims 3, 5, 7-11, 13-14, 16-18, 21-23:

These claims are rejected because they depend on claims 1, 12 and 19 and contain the same problems of indefiniteness.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. Claims 1-5, 9, 12-13, 15, 17-21 and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Garreau (6,425,101).

Claims 1, 3:

Garreau discloses the invention substantially as claimed. Garreau discloses (figures 2 & 4) a test network (200) including a master controller (202) connected to a programmable switch (204 or 408). The programmable switch (204) is connected to a slave target device (206) containing JTAG compliant integrated circuits (IC1 through IC4). The master controller (20) further comprises a JTAG controller (210) and a switch controller (218) for providing JTAG test protocols by using an I/O line (211-1) and data to the slave target device (206), and receiving the test results by using the feed backward line (211-2) via the programmable switch (204 or 408) (figures 2 & 4, column 4 lines 41-column 5 line 36).

Garreau does not explicitly teach the controllable switches. Garreau, however, teaches (figure 4) that the programmable switch (208) comprises a plurality of vertical data lines (402) and programmably connected to horizontal data lines (404) forming a "crossbar" switch. Each of the horizontal data lines (404) is connected to one of the programmable switch I/O lines (410). Each of the programmable switch I/O switch I/O lines (410) are in turn connected in a pair-wise manner to the ICs (IC1 through IC4) located on the target hardware device (206) such that each IC can be selectively tested (column 6 lines 49-column 7 lines 28).

It would have been obvious to one skilled in the art at the time the invention was made to realize that Garreau's combination of plurality of vertical data lines (402) and

the plurality of the horizontal data lines (404) (in Garreau's programmable switch [208]) would have been the controllable switches. One having ordinary skill the in the art would be motivated to realize so because Garreau's combination of vertical data lines (420) and horizontal data lines (404) are used for selectively connecting a IC [in the target device (206)] to the master controller (202) (column 7 lines 12-28).

Claim 2:

Garreau further teaches (figure 4) that the programmable switch (400) further comprises a connector (412-10) to connect a vertical data line (402-3) to the JTAG controller (210) by way of the I/O line (211-2) wherein the I/O line (211-2) feeds back the test results. The programmable switch (400) also comprises a connector (412-9) to connect the vertical data line (402)-4 to the JTAG controller (210) by way of the I/O line (211-2) (figure 4, column 8 lines 48-58; column 5 lines 10-36).

Claim 4:

Garreau further teaches (figure 4) that the programmable switch (400) further comprises a connector (412-10) to connect a vertical data line (402-3) to the JTAG controller (210) by way of the I/O line (211-2) wherein the I/O line (211-2) feeds back the test results. The programmable switch (400) also comprises a connector (412-9) to connect the vertical data line (402)-4 to the JTAG controller (210) by way of the I/O line (211-2). In this way the integrated circuits IC3 and IC2 can be tested and are daisy-chained in the JTAG path in responsive to the appropriate switch control signal from the switch controller (218) (figure 4, column 8 lines 32-58; column 5 lines 10-36).

Claim 5:

Garreau teaches (figure 7) a host computer (72) provides a user interface for sending corresponding configuration data to the master controller (704) then directs the programmable witch (706) to connect which of ICs (708 through 714) to be tested (figure 7, column 8 lines 57-column 9 line 5).

Claim 9:

Garreau teaches (figure 7) a host computer (72) provides a user interface for sending corresponding configuration data to the master controller (704) then directs the programmable witch (706) to connect which of ICs (708 through 714) to be tested (figure 7, column 8 lines 57-column 9 line 5).

Garreau does not explicitly teach a memory for storing the corresponding configuration data before sending such configuration data to the master controller (704). However, it would have been obvious to one skilled in the art at the time the invention was made to realize Garreau's host computer (702) would have comprised a memory for storing such configuration data. One having ordinary skill in the art would be motivated to realize so because having a memory for storing (configuration) data inside a computer (or a host computer) is well-known in the art.

Claims 12, 15 and 24-25:

Claims (12, 24, 25) and 15 are rejection for reasons similar to those set forth against claims (1 & 5) and 4, respectively.

Claim 13:

Garreau also teach that the horizontal data line controller (408) and the vertical data line controller (408), in responsive to the control signals, uses the connector (412-9) to connect the vertical data lines (402-4) by the way of the I/O line (211-1), and use the programmable connector (412-10) to connect the vertical data line (402-3) by way of the I/O line (211-1) (figure 5 lines (column 7 lines 37-54).

Claims 17 & 18:

Garreau's master controller (704) directs the programmable switch (706) to selectively couple an IC in responsive to the configuration data from the host computer (702) (figure 7, column 8 lines 62-622).

Claim 19:

Claim 19 is rejection for reasons similar to those set forth against claims (1 & 5) except that a memory with program software is recited. However, Garreau teaches (figure 7) that the host computer (702) provides executable instructions to a test network (703) (figure 7, column 8 lines 50-52).

Claims 20-21 & 23:

Claims (20 & 23) and 21 are rejection for reasons similar to those set forth against claims 15 and (17 & 18), respectively.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christine T. Tu whose telephone number is (571)272-3831. The examiner can normally be reached on Mon-Thur. 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571)272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Christine T. Tu
Primary Examiner
Art Unit 2138

February 27, 2006